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High mobility thin film transistors with indium oxide/gallium oxide bi-layer structures

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We investigate the transport properties of thin-film transistors using indium oxide (In_2O_3)/gallium oxide (Ga_2O_3) bi-layer stacks as the channel material. At low gate bias, we observe the transistor field-effect mobility increases with the film resistivity to $\mu_{FE} = 51.3$ cm^2/Vs and ON/OFF current ratio to 10^8 due to combinatorial layer thickness modulation. With the Ga_2O_3 layer thickness ratio increase to R = 14.35%, these observations are accompanied with one-order-of-magnitude reduction in the transistor subthreshold swing to 0.38 V/decade and suggest a trap-limited conduction mechanism upon which the reduced scattering centers due to annihilation of subgap states improve the device electric characteristics without post-growth annealing. © *2012 American Institute of Physics*. [doi:10.1063/1.3683518]

Thin film transistors (TFTs) are an essential element for flat-panel displays and next-generation microelectronic devices.[1] Hydrogenated amorphous silicon (a-Si:H) has been one of the widely used channel materials for TFTs. However, it suffers from issues such as low mobility ($\mu < 1$ cm^2/Vs) and instability under illumination and electric bias stress.[2] Alternative TFT channel design, comprising a superlattice structure made of hydrogenated silicon nitride (a-Si_3N_4:H)/a-Si:H, has been proposed to increase the mobility by a factor of 5 due to the quantization effect.[2] Recent study on amorphous indium-gallium-zinc-oxide (a-IGZO),[3] and their derivatives of a-IGO and a-IZO have drawn interest due to superior carrier mobility ($\mu > 10$ cm^2/Vs)[4] and low temperature processing.[5] Conventional wisdom suggests that the high carrier density in oxide semiconductors can be related to oxygen vacancies (V_O) and other native defects. Model analysis indicates that carrier transport is controlled by multiple trap-and-release events when the device is biased at *low* gate voltage with the Fermi level residing within the localized tail states.[6] The percolation conduction mechanism prevails when carriers are released to the non-localized states and find the paths of least resistance. Wave function overlap between the s-orbitals of the adjacent In cations can make the carrier transportation insensitive to structure disorder, thus leading to high field-effect mobility (μ_{FE}) in the oxide-based TFTs.[7] It was also noted that the formation energy of V_O increases with Ga atoms, which can suppress the O-deficiency related defects and improve device stability.[8,9] These observations outline a possibility to tailor the electric properties of oxide TFTs by adding Ga ions to enhance the material amorphization using the techniques such as sputtering[10] or solution-base process.[11]

Here, we demonstrate another aspect of engineering the transport properties of oxide TFTs by mitigating the trap density of subgap states (D_{sg}) in the In_2O_3/Ga_2O_3 bi-layer system. We note that as the Ga_2O_3 layer thickness ratio R, defined as $tGa_2O_3/(tGa_2O_3 + tIn_2O_3)$, increases from 11% to 25%, the equivalent film resistivity (ρ_{eff}) can span a wide range from 10^4 to 10^7 Ω cm with a rate of 5.35% $\pm$ 0.05%/decade. From bottom-gate TFTs made of such In_2O_3/Ga_2O_3 bi-layer stack, we achieve a peak field-effect mobility $\mu_{FE} = 51.3$ cm^2/Vs, ON/OFF current ratio of 10^8, and threshold voltage $V_T = 0.57$ V at a Ga_2O_3 layer thickness ratio R = 14.35% ($\rho_{eff} = 9.2 \times 10^4$ Ω cm). These data are taken *without* post-growth annealing and concurred with an order of magnitude reduction in the TFT subthreshold swing to S = 0.38 V/decade. Such behavior can be ascribed to a mechanism of suppression of subgap trap density D_{sg} in thin In_2O_3 layers when interfaced to Ga_2O_3.[8,9]

The preparation of In_2O_3/Ga_2O_3 bi-layer stack materials used in this study was facilitated by the sputtering method at a temperature below 60 °C. The materials were typically grown at a sputtering power of 70 W and working pressure of 4 mTorr, with flow rate of argon (Ar)/oxygen (O_2) fixed at 30/30 sccm (standard cubic centimeter per minute). Under these conditions, a growth rate of 0.14 Å/s and 0.09 Å/s, respectively, can be found for depositing the In_2O_3 and Ga_2O_3 films on quartz substrates. A transmission line method (TLM),[12] with electrode patterns composed of 200 nm-thick molybdenum (Mo) stripes of 4 to 16 μm spacing, was applied to characterize ρ_{eff}.

Shown in the inset of Fig. 1(a) are the resistance data taken on sample 1 designed to have 7 pairs of In_2O_3/Ga_2O_3 stack with 3.5/0.57 nm layer thickness in each pair. From a linear slope fitting of the resistance data to the Mo stripe spacing, one can extract ρ_{eff} by considering a multiplication factor of film thickness. This process allows us to examine the ρ_{eff} distribution associated with various In_2O_3/Ga_2O_3

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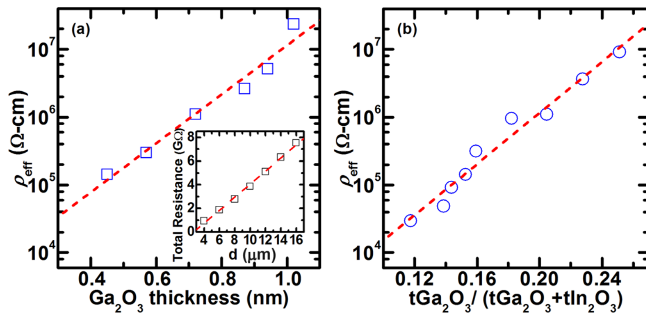

FIG. 1. (Color online) (a) The effective channel resistivity ($\rho_{\rm eff}$) for In_2O_3/Ga_2O_3 devices fixed with 3.5 nm-thick In_2O_3 but varied in the Ga_2O_3 layer thickness, inset: TLM data on device with 3.5/0.57 nm In_2O_3/Ga_2O_3, and (b) dependence of $\rho_{\rm eff}$ on the Ga_2O_3 thickness ratio according to the In_2O_3/Ga_2O_3 layer structures listed in Table I.

layer thickness combination. Referred to Fig. 1(a), logarithmic increase in $\rho_{\rm eff}$ at a rate of 5.35% ± 0.05%/decade is observed on samples fixed with 3.5 nm-thick In_2O_3 layers but varied in the Ga_2O_3 layer thickness. Similar increasing rate can also be found in Fig. 1(b) according to the In_2O_3/Ga_2O_3 layer thickness variation listed in Table I. With oxygen partial pressure *fixed* in our experiments, these analyses illustrate wide range of resistivity tunability (10^4 to 10^7 Ω cm) in the In_2O_3/Ga_2O_3 multi-layer system due to layer thickness modulation.

A plausible mechanism to the aforementioned phenomena is due to the mitigation of trap density of subgap states in the In_2O_3/Ga_2O_3 system.[8,9] The latter was examined by applying a high-low frequency capacitance analysis[13] to a metal insulator semiconductor capacitor (MIS-cap) device due to less parasitic circuit components than its TFT counterpart.[14] Two capacitor devices were prepared: MIS-cap A with a 30 nm-thick In_2O_3 *single* layer and MIS-cap B with an additional 2 nm-thick Ga_2O_3 layer deposited to In_2O_3 (Fig. 2(a)). These MIS-cap devices were fabricated on Mo-covered quartz substrates using 40 nm- and 200 nm-thick Si_3N_4 and Mo layers as the insulator and top/bottom electrodes. Here the low-frequency (lf, 50 Hz) and high-frequency (hf, 100 KHz) capacitance data were measured as a function of the bias voltage and normalized to that ($C_i = 17.9$ pf) of Si_3N_4 gate capacitance. A first glance of data shown in Fig. 2(b) depicts a positive shift of the C-V curves of MIS-cap device B to those of MIS-cap device A. It reveals a combined effect due to change in the flat-band voltage and work function difference in the single-layer In_2O_3 and bi-layer In_2O_3/Ga_2O_3 structure.[13] Stretch-out of the high-frequency C-V component with respect to its low-frequency counterpart signifies a subtlety that the interfacial traps/charges do not follow the high-frequency modulation signal such that the capacitance value slowly varies with the gate bias (V_G).

One can further extract the interfacial trap density D_{it} with Eq. (1),[13] where C_i is the insulator (Si_3N_4) capacitance and C_{lf}/C_{hf} the low/high frequency, respectively.

$$D_{it} = (1/q)\{[(1/C_{lf}) - (1/C_i)]^{-1} - [(1/C_{hf}) - (1/C_i)]^{-1}\}. \quad (1)$$

Referred to the inset of Fig. 2(b), our analysis indicates that an order of magnitude reduction in the peak value of D_{it}, varying from $\sim 2 \times 10^{13}$ to $\sim 2 \times 10^{12}$ eV^{-1} cm^{-2} at $V_G > 0$, can be achieved when a 2 nm-thick Ga_2O_3 layer is added to an In_2O_3 MIS-cap device.

These observations highlight a promising use of In_2O_3/Ga_2O_3 bi-layer channel for TFT operation. As a proof, another set of TFTs was fabricated according to the layer thickness variation listed in Table I. A device cross-sectional view is shown in the inset of Fig. 3(a). First, the quartz substrate was etched to a depth of ~70 nm followed by Mo-layer deposition which serves as the bottom-gate electrode. A 9 nm-thick hafnium oxide (HfO_2) layer was then deposited on the Mo-covered quartz substrate using an atomic layer deposition method. The drain/source contacts were made of 200 nm-thick Mo layers. The device surface was passivated with 100 nm-thick SiO_2 and a layout of 4 μm gate length (L_g) and 80 μm gate width (L_W) was used for electric characterization.

Illustrated in Fig. 3(a) are the representative output characteristics of TFT sample C having a Ga_2O_3 layer thickness ratio R = 14.35%, corresponding to nominal single layer thickness of $In_2O_3 = 3.71$ nm, $Ga_2O_3 = 0.63$ nm and $\rho_{\rm eff} = 9.2 \times 10^4$ Ω cm. We denote linear increase in the drain-to-source current (I_{DS}) with respect to V_{DS}, followed by pinch-off and saturation of I_{DS} with further increase of V_{DS}. From the log-plot of transfer curve in Fig. 3(b), one can denote an ON/OFF current ratio of 1×10^8 and a subthreshold swing of S = 0.38 V/decade. One can further take advantage of the linear I_{DS}-V_{GS} characteristics to evaluate the transistor threshold voltage.[15] This was taken by linear interpolation of the I_{DS} curve to intersect the V_{GS} axis at $I_{DS} = 0$, which procedure shown in the inset of Fig. 3(b) renders $V_T = 0.57$ V. One can further extract the transistor transconductance (g_m) according to $g_m = \partial I_{DS}/\partial V_G$. It can facilitate the derivation of field-effect mobility μ_{FE} for TFT

$$\mu_{FE} = (L_g \times g_m)/(L_W \times C_{OX} \times V_{DS}) \quad (2)$$

This scenario leads to an increase of g_m with V_{GS} where maximum value of $g_{m,max} = 277.2$ μS can be observed at

TABLE I. Summary of the equivalent film resistivity and current ON/OFF ratio for TFT devices studied in Figs. 1(b) and 4 with various In_2O_3/Ga_2O_3 thickness combination.

TFT	tIn_2O_3 (nm)/tGa_2O_3(nm)	Resistivity (Ω cm)	I_{ON}/I_{OFF} ratio	TFT	tIn_2O_3 (nm)/tGa_2O_3(nm)	Resistivity (Ω cm)	I_{ON}/I_{OFF} ratio
A	4.06/0.54	2.46×10^4	10	F	3.64/0.81	9.58×10^5	1.3×10^4
B	3.92/0.63	4.88×10^4	1.0×10^5	G	3.50/0.90	1.10×10^6	1.0×10^4
C	3.71/0.63	9.20×10^4	1.0×10^8	H	3.36/0.99	3.68×10^6	1.0×10^4
D	3.50/0.63	1.43×10^5	4.8×10^7	I	3.22/1.08	9.20×10^6	1.1×10^4
E	3.80/0.70	3.10×10^5	6.0×10^5				

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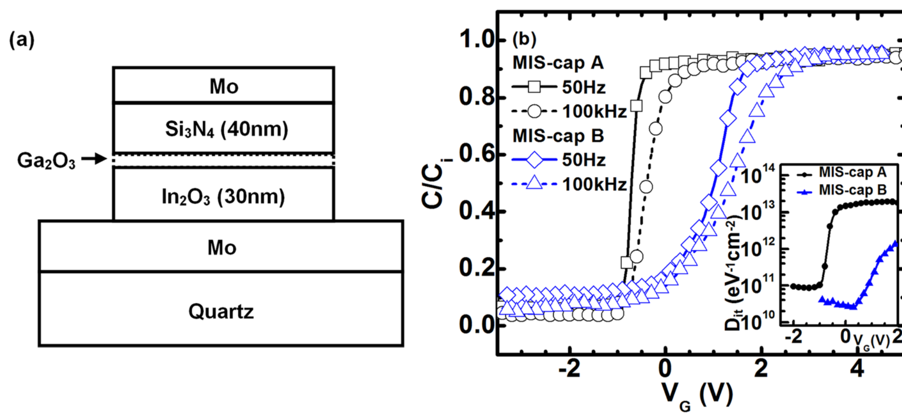

FIG. 2. (Color online) (a) Schematic layout of the MIS-capacitor sample B with 2 nm/30 nm Ga_2O_3/In_2O_3. (b) High and low C-V data on MIS-capacitor samples A/B and normalized to the Si_3N_4 gate capacitance ($C_i = 17.9$ pf). Inset: extracted interfacial trap charge density (D_{it}) as a function of gate bias.

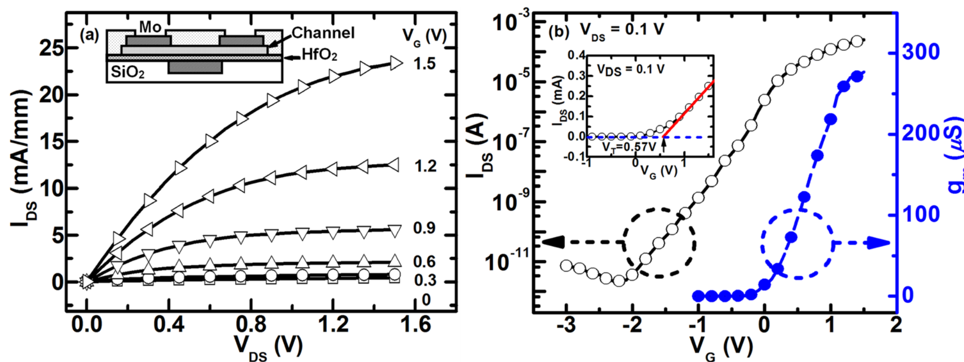

FIG. 3. (Color online) (a) Output and (b) transfer characteristics for In_2O_3/Ga_2O_3 TFT sample having an equivalent film resistivity $\rho_{eff} = 9.2 \times 10^4\ \Omega$ cm and Ga_2O_3 layer thickness ratio R = 14.3%. Inset: (a) schematic layout of the TFT structure, (b) the extraction of threshold voltage.

$V_{GS} = 1.5$ V and $V_{DS} = 0.1$ V. Continued with parameter extraction using dielectric constant $\varepsilon_r = 27.9$ for HfO_2 and $C_{ox} = 2.7\ \mu F/cm^2$ in Eq. (2), μ_{FE} of 51.3 cm^2/Vs can be derived at $L_g/L_W = 4\ \mu m/80\ \mu m$.

Further compiled in Fig. 4 are the extracted data of μ_{FE} for devices designed to have various Ga_2O_3 layer thickness ratio R and hence difference in the film resistivity (ρ_{eff}). The data were taken *without* post-growth annealing and measured at a low bias condition of $V_{GS} = 1.5$ V and $V_{DS} = 0.1$ V. Here, we denote an initial increase of μ_{FE} with ρ_{eff} in the low-resistivity (10^4–10^5 Ω cm) regime, reaching a peak value of 51.3 cm^2/Vs at $\rho_{eff} = 9.2 \times 10^4\ \Omega$ cm, followed by rapid drop of μ_{FE} down to 5-10 cm^2/Vs in the high-resistivity

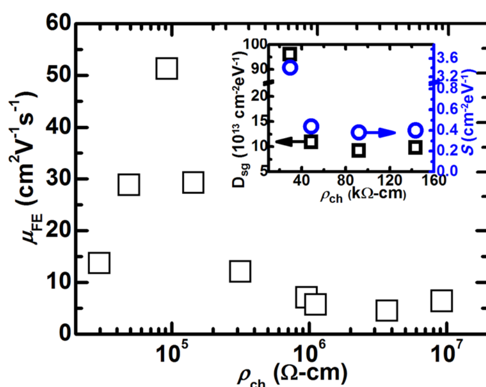

FIG. 4. (Color online) Dependence of field-effect mobility (μ_{FE}) in In_2O_3/Ga_2O_3 TFTs having various Ga_2O_3 layer thickness ratio R. Inset: the subthreshold swing S and the extracted trap density of the subgap states D_{sg} for devices at low gate bias ($V_{GS} = 1.5$ V) and in the low resistivity regime (<10^5 Ω cm).

(10^6–10^7 Ω cm) regime. Similar behavior in the μ-ρ relation has been reported in the solution-processed In_2O_3 TFTs annealed in air or in an O_2/O_3 ambient,[16] or in the tin doped In_2O_3 films deposited with various oxygen partial pressure.[17] Indeed the peak value of $\mu_{FE} = 51.3\ cm^2/Vs$ observed in this work is comparable to that of In_2O_3 TFT annealed at 500 °C,[16] or in the doped In_2O_3 film,[17] operated at a much large gate bias condition ($V_{GS} > 15$ V). In comparison, our study on 50 nm-thick IGZO TFT with $2.8 \times 10^4\ \Omega$ cm film resistivity and thick 35 nm-HfO_2/15 nm-SiO_2 bottom-gate dielectric exhibits low value mobility ~8.9 cm^2/Vs and high voltage operation characteristics of $V_{DS} = 6$ and $V_{GS} = 8$ V.[18]

We further note that in the low resistivity regime (<10^5 Ω cm), increase of μ_{FE} is accompanied with an order of magnitude reduction in the transistor subthreshold swing (S) from 3.4 to 0.38 V/decade and improved ON/OFF current ratio from 10 to 1×10^8 (data listed in Table I and inset of Fig. 4). Indeed, by correlating the trap density of subgap states (D_{SG}) to the measured S value according to[15]

$$S = \ln 10 \cdot (k_B T/e) \cdot (1 + eD_{SG}/C_{OX}), \tag{3}$$

one can discern D_{SG} reduction from 9.6×10^{14} to $9.2 \times 10^{13}/cm^2$ eV. Under the *low* gate bias condition, these observations signify a trap-limited transport mechanism[6] upon which the reduced scattering centers due to annihilation of subgap states in the $HfO_2/In_2O_3/Ga_2O_3$ bi-layer channel increases the device mobility and improve the ON/OFF current ratio.[17] Compared with our recent work on thick-dielectric HfO_2/SiO_2/IZGO TFT,[18] it reveals the advantages of using thin high-k dielectric to reduce the operation voltage and thin Ga_2O_3 layers to suppress D_{sg} and enhance μ_{FE}.

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In summary, we demonstrated a device concept using the layer thickness modulation in an In_2O_3/Ga_2O_3 bi-layer stack channel to achieve enhancement mode operation of TFT ($V_T = 0.57$ V) with high field-effect mobility ($\mu_{FE} = 51.3$ cm^2/Vs), low subthreshold swing (S = 0.38 V/dec) and ON/OFF current ratio of 10^8. At low gate bias and low resistivity regime, these observations are ascribed to a trap-limited transport mechanism upon which the reduced trap density of the subgap states dominates in the device electric properties.

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